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Abstract

This paper investigates the aging of a 650V, 30A GaN HEMT power transistor under operational switching conditions. The switching stress respects the Safe Operation Area (SOA) of the tested transistor. The aging campaign lasted 1008h and was carried out through a developed switching application with high power efficiency. The global aging results show the degradation of five parameters: drain current I_D, on-state resistance $R_{DS(ON)}$, transconductance g_m, gate leakage current I_{GSS}, and threshold voltage V_{TH}. The major causes that affect the reliability of the GaN HEMT are hard switching, long time of test and high intensity of the stress. The existence of trapped charge in the gate-drain access region after aging is demonstrated using pulsed measurements. The effects of this degradation on power converters are studied by modeling the static characteristics of the aged GaN HEMT using an accurate method based on the Levenberg-Marquardt Algorithm. The accuracy and consistent convergence of the developed SPICE model provide a good way to investigate the reliability of GaN HEMTs by a simulation approach.

1. Introduction

Investigating the reliability of GaN HEMT is receiving an increasing interest from research laboratories worldwide. The attention of academics and industrials on reliability of GaN HEMT is accelerated by the impressive growth of GaN HEMTs market, due to their high superior performances compared to those of Silicon power transistors. Their applications are in various domains, such as green energy and RF engineering.

To validate the robustness of GaN HEMTs power transistors, JEDEC standardized tests for Si power transistors are used [1]. However, the standardized tests for Si are not enough to guarantee the robustness of GaN transistors when they are used in power converter applications, because the reliability of GaN under switching operation is different from that of Si transistors [2]. Moreover, running GaN HEMTs power transistors under accelerated conditions would cause many non-GaN failures.

In the literature, the reliability of GaN HEMTs has been improved. Reference [3] classifies the degradation modes of GaN HEMT in switching mode DC power converter into three classes: on-state, off-state and semi-off state. According to [4], one of the major disadvantages limiting the reliability of GaN HEMTs for switching power applications is hot electron effects that occurs during the switching state. In [5], this degradation result in decreased DC and RF performance.

According to [6], it is important to study the reliability of GaN HEMT for power conversion circuits. This paper presents a developed reliability methodology under operational switching conditions. The proposed aging switching bench presents high power efficiency. The effects of aging GaN HEMT transistor on a power converter application are studied by SPICE simulation approach.

In this paper, we studied the effects of aging GaN HEMT power transistor under switching conditions at high current and low voltage. However, other aging profiles at low current and high voltage or combined high voltage and high current are necessary to completely understand the degradation mechanisms of GaN HEMT power transistors under switching conditions.

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2. Methodology

Tested transistor is a fresh GS66508P from GaN Systems [7], which is a p-type gate normally-off AlGaN/GaN power transistor operating in the range of 650V/30A. In the following lines, the aged GaN HEMT transistor will be noted DUT_M. The evolution of the electrical parameters of the DUT_M from the new state to the aged state is monitored using a pulsed I-V measurements at a pulse frequency of 100 Hz and a pulse width of 4 µs, which is short enough to ensure iso-thermal measurement of pulsed I-V GaN HEMT characteristics. Moreover, to separate trapping effects on measurements, pulsed I-V characteristics were performed at DC-bias levels V_{GS0}=0 and V_{DS0}=0. At this bias condition, trapping is expected to be negligible.

During aging, five DC characteristics were measured successively at the fresh state (t = 0), 144h, 312h, 456h and 1008h. The first four characterizations are separated by an average of 150h, which is short enough to ensure a regular aging monitoring in the infant stage [8]. The fifth characterization is performed after 500h before the last one so that the aging process is not interrupted and thus the degradations of the device can be detected.

Fig. 1 shows the developed aging switching bench, which is described in [9]. The gate driver proposed in [10] has been used to drive the power GaN HEMTs. PWM1 and PWM2 are two complementary pulse width modulated signals. The proposed switching circuit enables to investigate the impact of hot electrons on GaN HEMTs with low energy consumption compared to that in [11] because no load is used. The used switching conditions presented in Table 1 have been chosen to ensure that the DUT_M switches under its Safe Operating Area (SOA). As can be seen in Fig. 2, the developed switching bench places similar stresses on the DUT_M, which could exist in a large class of power management products such as power converters: on-state stress, semi-off state stress and off-state stress. In the on-state, DUT_M is on, I_D is equal to 14A and V_{DS} is equal to 1.14V. In the semi-off state, DUT_M is turning-on, when both high current and high voltage exist simultaneously. In the off-state, DUT_M is off, I_D is null and V_{DS} is equal to 24V. The current rise time is equal to 3.94 µs and the voltage rise time is equal to 53.46 ns. To ensure that the aging of the DUT_M respects the SOA, the measurements of the junction temperature T_J, I_D current and V_{DS} voltage are performed.

2.1. I_D current and V_{DS} voltage limitations

At the on-state, the I_D current is equal to 14A. At the off-state, the V_{DS} voltage is equal to 24V. The use of high drain-source bias (in off-state) may favor the trapping of electrons under the gate and/or in the gate-drain access region. This results in an increase of the dynamic on-resistance $R_{dyn(on)}$. Thus, the choice of a high drain current (I_{DS} = 14A) and a low drain-source voltage (24V) enables to separate degradations caused by thermal dissipation from that caused by high electric field. Nevertheless, the investigation of the effect of high electric field on GaN HEMT is mandatory to distinguish experimentally between the degradations caused by self-heating mechanism at high current and low voltage, and those caused by high voltage switching conditions as well.

According to the SOA of the DUT_M in [7], it can be seen that the used 14A, 24V pulse (see Table 1) is located below the 10µs line limit. This indicates that the pulse is placed within acceptable limits of I_D and V_{DS} given by the constructor.

2.2. Junction temperature limit

Under the switching conditions in Table 1, the temperature T_J is estimated using the thermal model of DUT_M package mounted on a PCB and a heatsink described in [12]. By using the thermal Ohm's law:

$$T_J = P_{tot} \cdot \theta_{JA} + T_A \quad (1)$$

Where Θ_{JA} is the total thermal resistance from junction to ambient, which is equal to 3.63°C/W based on both manufacturer datasheets and SPICE model, T_A is the ambient temperature fixed at 25°C by heatsink cooling, and P_{tot} is the experimental total power loss of DUT_M over one period in watts, which is calculated by

$$P_{tot} = \frac{1}{T}\int_0^T i_{ds} \cdot v_{ds} \cdot dt \quad (2)$$

Where, T is the period, i_{ds} and v_{ds} are the instantaneous drain current and drain-source voltage, respectively.

From experimental measurements (Fig. 2), P_{tot} is equal to 16.68 W, the corresponded T_J is calculated using (1) and is equal to 86 °C, which is below the allowable T_J limit of 150°C. Once the switching conditions are fixed, the effect of aging

the GaN HEMT under switching safe operational conditions can be investigated.

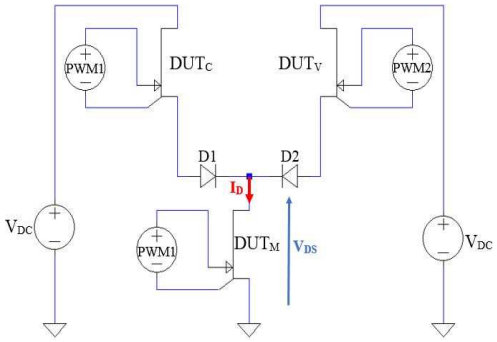


Fig. 1. Aging switching bench

Table 1
Applied switching conditions on DUT_M

$V_{DS(OFF)}$	$V_{DS(ON)}$	I_{DS}	frequency	t_{pulse}	duty-cycle
24 V	1.14 V	14 A	50 kHz	10µs	50%

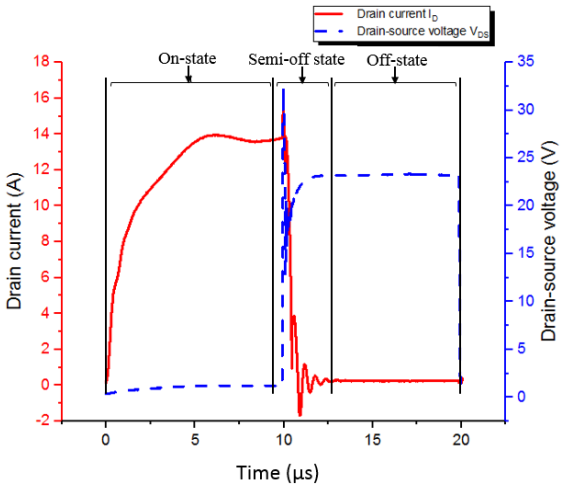


Fig. 2. I_D and V_{DS} waveforms of DUT_M over one period for switching conditions: 50 kHz, duty-cycle = 50%, and 14A/24V operating conditions.

3. Results and analysis

The on-state resistance $R_{DS(ON)}$ is calculated in the linear region of the I_{DS}-V_{DS} characteristic, using (3).

$$R_{DS(ON)} = \left.\frac{\Delta I_D}{\Delta V_{DS}}\right)^{-1}_{V_{GS}=6V,V_{DS}\to 0V} \quad (3)$$

Fig. 3 shows the evolution of $R_{DS(ON)}$ during 1008h of aging under the switching conditions described in Table 1. As can be seen, $R_{DS(ON)}$ increases by 27.11% after aging. According to [13], the observed increase of $R_{DS(ON)}$ is ascribed to trapping of hot electrons in the gate–drain access region during semi-off state. The trapping of electrons in the buffer due to the off-state bias may also induce the increase of $R_{DS(ON)}$. This may lead to the increase of power conduction losses and thus the device temperature elevation, resulting in reduced power GaN HEMTs efficiency and lower DC performances.

The transconductance g_m is defined as the maximum first derivative of the input characteristic in the saturation region. Fig. 3 shows the evolution of g_m during 1008 h of aging under the switching conditions presented in Table 1. The resulted g_m after aging is reduced by 9.88% compared to its values before aging. The decrease in g_m is mainly due to the presence of hot electrons caused by the semi-off state, when both channel current and high electric field are present in the device [14], which could generate defects typically highest at the end of the gate on the gate–drain side [15], resulting in reduced RF performances.

The drain current I_D is determined from the measured I_{DS}-V_{DS} static characteristic at V_{GS} = 6V and V_{DS} = 0.76V. Fig. 4 shows the evolution of the current I_D during 1008h of aging under the switching conditions described in Table 1. As can be noticed, I_D decreases by 22.33% after aging. This phenomenon is called current collapse, where I_D is reduced due to hot electrons during switching [16]. The reduction in I_D after aging can be observed in the I_D-V_{GS} static characteristic (Fig. 5). According to [17], the current collapse can be suppressed by hole injection from drain.

From Fig. 6, the existence of trapped charge after aging in the gate-drain access region is experimentally demonstrated by pulsing from various quiescent voltages (V_{GSQ};V_{DSQ}): (0;0), (-8V;100V) and (-8V;300V). The exposition to both a negative V_{GSQ} and a high V_{DSQ} fosters the trapping of electrons in the drain access region of the DUT_M, while the reference condition is V_{GSQ}=0V and V_{DSQ}=0V. Measurements were carried out at 25 ◦C in the dark.

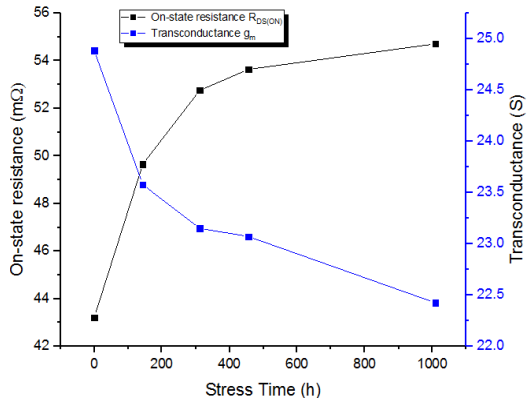


Fig. 3. Evolution of $R_{DS(ON)}$ and g_m during 1008 h of aging

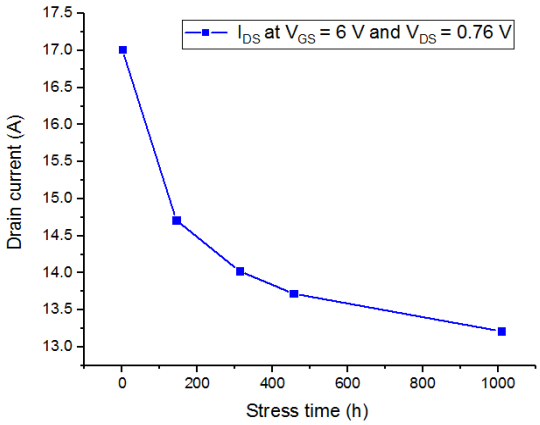


Fig. 4. Evolution of the drain current measured at V_{GS} = 6 V and V_{DS} = 0.76 V

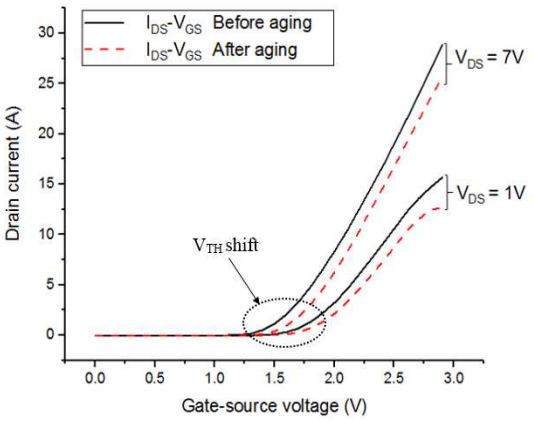


Fig. 5. I_{DS}-V_{GS} characteristics measured at V_{DS} equals to 1V and 7V

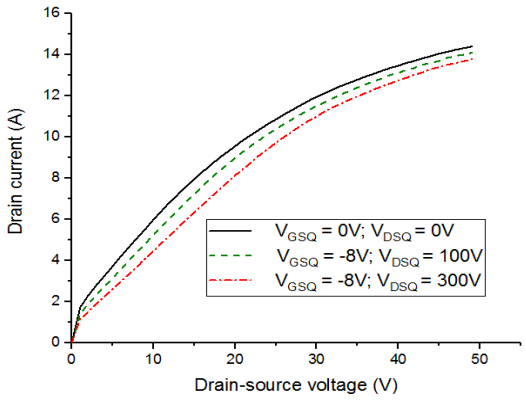


Fig. 6. I_{DS}-V_{DS} characteristics for various quiescent bias points at 25°C in the dark.

From Fig. 5, a small shift of the threshold voltage V_{TH} is observed. Before aging V_{TH} was equal to 1.81V this value rises to 1.89 V after aging, with an increase of 4.17%. The small shift of V_{TH} voltage is also noticed in [18]. According to [19], the negative shift of V_{TH} is due to the creation of defects under the gate caused by hot electrons during semi-off stress. In reference [20], the charge trapping at the pGaN/AlGaN interface due to the bias-temperature instability (BTI) may also produce the shift of the V_{TH}.

Moreover, a negligible increase in the gate current leakage is measured using Keithly 2636B SourceMeter, we found that I_{GSS} was equal to 11.69 µA before aging and equals to 12.08 µA after aging. The slight increase in I_{GSS} current is also confirmed in [21]. As presented in [22], the resulted degradation of I_{GSS} current is attributed to the generation of defects/leakage paths in the p-type/AlGaN gate interface due to hot electrons.

Table 2 summarizes the values of $R_{DS(ON)}$, g_m, I_D, V_{th} and I_{GSS} before and after 1008h of aging DUT_M under the switching conditions presented in Table 1. The re-measurement of the static parameters after a long relaxation period shows no reversibility of the phenomena. The absolute relative degradation can be calculated by

$$Degradation(\%) = \frac{(x_b - x_a)}{x_b} \qquad (4)$$

Where x_a and x_b are the DUT_M parameter values after and before aging respectively.

4. Modelling aging

The purpose of this part is to model the aging of the DUT_M in order to evaluate the effects of aging the GaN HEMT under SOA on the power efficiency of the DC-DC converters by a SPICE simulation approach. To remain the same switching

conditions of the studied aging campaign, a 24V converter application is used. Fig. 7 shows the studied DC-DC converter, which is a 12/24 V boost converter with an output power equals to 180 W. The DUT_M is the SPICE model of the aged GaN HEMT.

The proposed drain current model of DUT_M is a non-segmented, smooth and continuous equation inspired from the Motorola Electrothermal Model (MET) [23], the specific equation is shown as follows:

$$I_{DS} = K \cdot \log\left[1+\exp\left(\frac{V_{GS}-b}{c}\right)\right] \cdot \frac{(m+n\cdot V_{GS})V_{DS}}{1+P\cdot(d+e\cdot V_{GS})V_{DS}}, V_{DS} \geq 0 \quad (5)$$

Where K is the device forward transconductance parameter at 25°C, P is the output conductance at 25°C, b and c are related parameters of the transfer characteristic, while m, n, d and e are related parameters of the output characteristic. The different parameters are extracted using an accurate method based on the Levenberg-Marquardt algorithm, which is described in [24].

Table 2
1008 hours aging results for DUT_M.

	$R_{DS(ON)}$ (mΩ)	gm (S)	I_{DS} (A)	V_{th} (V)	I_{gss} (µA)
t = 0	43.04	24.88	17.01	1.81	11.69
t = 1008 h	54.71	22.42	13.21	1.89	12.08
Degradation(%)	27.11	9.88	22.33	4.17	3.16

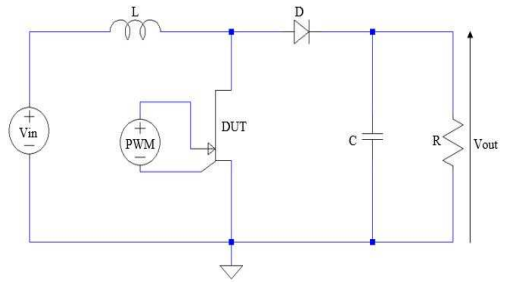


Fig. 7. DC-DC boost converter, with L = 76.8 µH, C = 1.25 µF and R = 3.2 Ω, at 50 kHz switching frequency, 12V input voltage and 24V output voltage.

The extracted static model parameters at 25°C for the fresh state (t =0) and the aged state (t = 1008h) are shown in Table 3. From the extracted parameters in Table 3, the modelled output and transfer characteristics of DUT_M before and after 1008h of aging are shown in Fig. 8. As can be observed, the developed aged SPICE model shows good convergence compared to experiment. The fresh and aged models of the DUT_M are implemented using LTspice simulator.

The conduction power losses P_C is calculated by

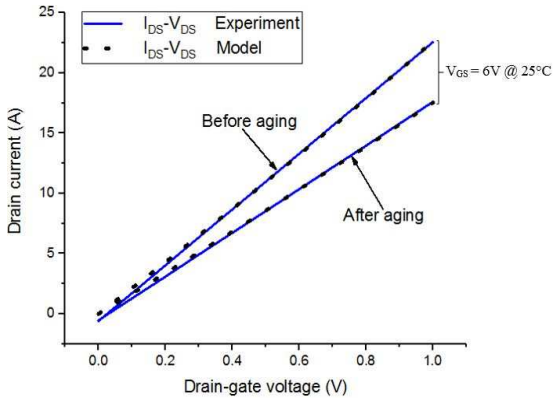
$$\begin{cases} P_C = \dfrac{1}{T_{on}} \displaystyle\int_{t=0}^{T_{on}} i_{ds} \cdot v_{ds} \cdot dt \\ T_{on} = \dfrac{d_c}{f} \end{cases} \quad (6)$$

Where T_{on} is the conduction time, dc is the duty cycle and f is the frequency.

Figure 9 shows the measurement of P_C at three output currents in the studied DC-DC boost converter. From Fig. 9, the effect of aging the GaN HEMT in the SOA during 1008h is that it produces an increase of P_C losses after aging. The increase of P_C is due to the increase of the DUT_M on-state resistance after aging. Resulting in decreased power converter efficiency. From table 4, an average increase of P_C equals to 8.82% is observed between the before aging state and the after aging state for various output currents: 14 A, 16 A and 18 A.

Table 3
Extracted Static Model Parameters at 25°C for the Fresh State (t = 0) and Aged State (t = 1008h)

	K	P	b	c	m	n	d	e
t=0	2.24	0.58	1.69	0.16	6.39	-0.92	2.59	-0.44
t=1008h	0.76	0.39	1.74	0.12	11.63	-1.68	3.21	-0.55



(a)

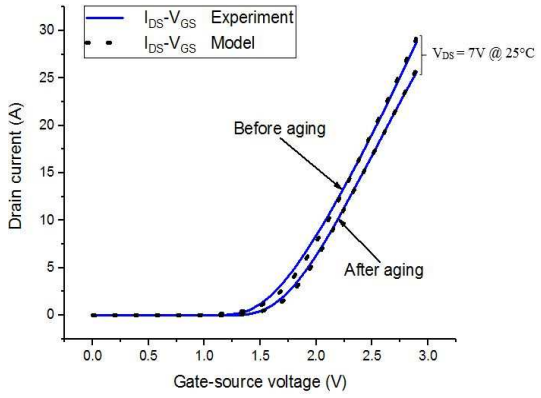


Fig. 8. Experiment and model (a) Output characteristics I_{DS}-V_{DS}; (b) transfer characteristics I_{DS}-V_{GS} before and after 1008h of aging.

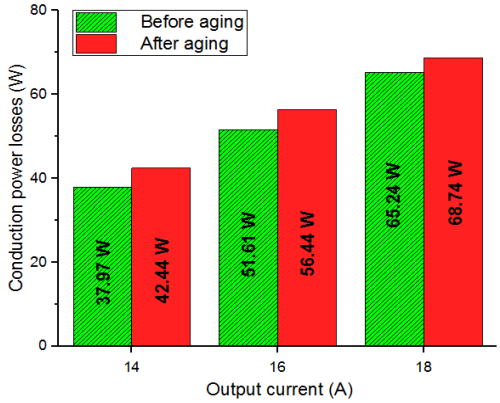


Fig. 9. Conduction power losses of DC-DC boost converter before and after aging for different output current: 14A, 16A and 18A.

Table 4
DC-DC boost converter conduction power losses, before and after aging for output current: 14A, 16A and 18A.

P_C (W)	14A	16A	18A
Before aging (t=0)	37.97	51.61	65.24
After aging (t=1008h)	42.44	56.44	68.74
Degradation (%)	11.77	9.35	5.36

5. Conclusion

This paper investigates the reliability of GaN HEMT power transistor under operational switching conditions, which could exist in a large class of power management products such as power converter. The switching conditions respect the safe operating area of the tested device given by the constructor, which provide a useful information about the degradation of GaN HEMT transistor under use conditions. The proposed switching bench gives an efficient way with low power consumption to study the reliability of power GaN HEMT under switching conditions. The aging campaign lasted 1008h and it has resulted on a degradation of the static parameters $R_{DS(ON)}$, g_m, I_D, V_{th} and I_{GSS} which is attributed to the hot electron generated during the switching state. The existence of trapped charge in the gate-drain access region after aging is experimentally demonstrated by pulsing from various quiescent voltages. Also, we studied the effect of aging GaN HEMT on the efficiency of a DC-DC power converter by a simulation approach. For next, we will perform others switching campaigns at various switching frequencies to study the effect of hard switching on power converters with GaN HEMT transistors.

Acknowledgment

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