Impact of the in situ SiN Thickness on Low-Frequency Noise in MOVPE InAlGaN/GaN HEMTs

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Impact of the *in situ* SiN thickness on low frequency noise in MOVPE InAlGaN/GaN HEMTs

M. Rzin, B. Guillet, L. Méchin, P. Gamarra, C. Lacam, F. Medjdoub and J-M. Routoure

***Abstract*—This paper reports on sub-10 nm quaternary barrier InAlGaN/GaN High Electron Mobility Transistors (HEMTs) grown by Metal-Organic-Vapor-Phase-Epitaxy (MOVPE) with an *in situ* SiN passivation layer, and ultra-short gate length of 200 nm. Two batches of HEMTs with two SiN thicknesses (t_{SiN}) of 14 and 22 nm are studied. Low Frequency Noise (LFN) measurements of the drain current have been carried out in the linear regime and showed that the *in situ* SiN thickness has no impact on the noise performance. S_{ID}/I_D^2 in the linear regime dependence over the gate overdrive shows that the channel noise is located under the gate and that the noise is not impacted by the thickness of the *in situ* SiN layer.**

***Index Terms*—InAlGaN/GaN, *in situ* SiN passivation, low frequency noise, HEMT**

I. INTRODUCTION

ULTRA-THIN quaternary barrier InAlGaN/GaN High Electron Mobility Transistors (HEMTs) hold a tremendous potential for microwave and millimeter-wave applications, thanks to their outstanding 2-DEG properties that allowed to achieve state of the art electron mobility of 1800 $cm^2 \cdot V^{-1} \cdot s^{-1}$ and sheet carrier density of $1.9 \cdot 10^{13}$ cm^{-2} at room temperature [1]. This is owing to the use of Al-rich InAlGaN layers having an important effect to enhance the carrier density and achieve high frequency performance due to the increase of the spontaneous polarization [2]-[6].

One of the critical parameters limiting dynamic and power performance as well as the electrical reliability of GaN based HEMTs is the gate leakage current that might increase under high electric field [7]-[9]. The parasitic effects leading to current collapse and gate leakage current increase have been reduced by using deposited SiN passivation [10]-[12]. However, the leakage current remains a serious issue when ultra-thin barrier layers are used. In order to reduce the leakage current under the gate and/or in the gate-drain access region, the deposition of an *in situ* SiN passivation layer on top of the quaternary barrier in the Metal-Organic-Vapor-Phase-Epitaxy (MOVPE) reactor has been proposed and successfully applied.

The passivation layer deposited in the same growth run as the III-N heterostructure reduces the relaxation, cracking and surface roughness of the barrier layer [13]. Moreover, the low growth rate and the relative high growth temperature of *in situ* SiN layer reduce the formation of surface states and improve the performance of the 2DEG properties.

The thickness of *in situ* SiN dielectric gate has a significant impact on the leakage current and may affect the drain current. Thick SiN cap increases the distance between the channel and the surface, thus reducing the surface state effects. On the other hand, much larger SiN cap makes the definition of ultra-short gate footprints more challenging.

Low frequency noise (LFN) measurements can be used to investigate the material/device quality, to identify material defects and trapping effects, and to investigate the reliability of GaN based HEMTs [14]–[18]. In addition to significant reduction of the gate leakage current and the increase of the sheet charge density, the *in situ* SiN passivation layer can also potentially improve the low frequency device noise performance [19]-[23].

In this letter, we report on low frequency noise measurements performed on InAlGaN/GaN HEMTs with different MOVPE *in situ* SiN passivation thicknesses.

II. EXPERIMENTAL DETAILS

The SiN/InAlGaN/GaN HEMT structures were grown in an Aixtron Close Coupled Showerhead (CCS) MOVPE reactor on 4H-SiC semi-insulating substrates.

The growth details were published in Ref. [24]. First SiC substrate surfaces were prepared in H_2 and the growth was initiated with an AlN nucleation layer (100 nm thick) at high temperature. A 1.6 μm thick highly resistive carbon doped GaN buffer layer, a 150 nm thick non-intentionally doped GaN channel, an AlN interlayer with a nominal thickness of 1.2 nm and a 6 nm thick InAlGaN barrier layer were subsequently deposited. It was checked by STEM-EDS (Scanning Transmission Electron Microscopy – Energy-Dispersive Spectrometry) and μ-Auger analyses that the

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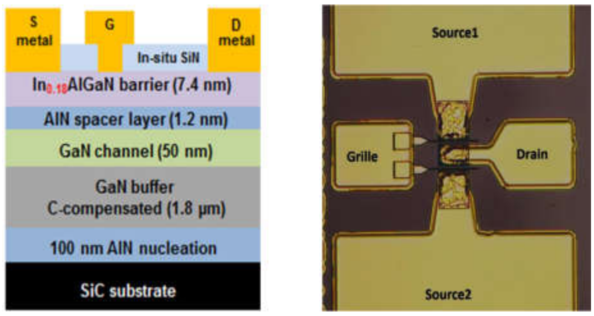
quaternary barrier showed Ga content of about 8–10% and In content ranging from 10% to 12%. At last, the SiN passivation layer (14 nm or 22 nm, noted t_{SiN}) was deposited on top of these heterostructures without growth interruption. Scanning Probe Microscopy (SPM) in conductive mode shows that the targeted thicknesses for the passivation layers are sufficiently thick to act as insulating layers. Device processing was performed as follows: ohmic contacts were formed directly on top of the InAlGaN barrier layer by etching the in situ Si_xN_y layer using a Fluorine-based plasma. A Ti/Al/Ni/Au metal stack was used, followed by rapid thermal annealing at 875 °C. Device isolation was achieved by nitrogen implantation. Ohmic contact resistances extracted from linear transmission line model (TLM) structures were 0.3 Ω.mm on average. A Ni/Au T-gate of 200 nm (L_G) was defined by e-beam lithography. Finally, a 200 nm thick SiN layer has been deposited as passivation.



(a) *(b)*

Fig. 1. (a) Schematic cross-section view and (b) optical microscope image of SixNy/InAlGaN/AlN/GaN HEMT with 2 finger gates.

In this work, the studied devices have a Ni/Au T-gate of 200 nm length (L_G) with two finger gates of width W_G = 25 µm. and 3 different gate drain region spacings L_{GD} (1, 2 and 3 µm). The schematic cross-section view and an optical microscope image of the HEMT heterostructure are displayed in figure 1.

III. RESULTS AND DISCUSSION

Typical I_D-V_{GS} and g_m-V_{GS} characteristics at V_{DS} = 200 mV in the linear regime of two representative InAlGaN/GaN HEMTs (A) with t_{SiN} = 14 nm and L_{GD} =1, 2 and 3 µm are shown in Fig.2. The threshold voltage is around -1.6 V. These devices have an electron mobility of 1792 $cm^2 \cdot V^{-1} \cdot s^{-1}$ and sheet carrier density of $1.64 \cdot 10^{13}$ cm^{-2}, resulting in a sheet resistance of 212 Ω/□. Fig. 3 shows I_D-V_{GS} and g_m-V_{GS} characteristics of two representative InAlGaN/GaN HEMTs (B) with t_{SiN} = 22 nm and L_{GD} = 2 and 3 µm. The threshold voltage is around -2.2 V. These devices have an electron mobility of 1772 $cm^2 \cdot V^{-1} \cdot s^{-1}$ and sheet carrier density of $1.60 \cdot 10^{13}$ cm^{-2}, resulting in a sheet resistance of 220 Ω/□.

The gate and drain subthreshold leakage currents are between 1 and 10 µA/mm at V_{GS} = -5V and V_{DS} = 10 V, typical of the Schottky contact on GaN based HEMTs. The main difference between A and B HEMTs is the negative shift of the threshold voltage when increasing the SiN thickness from 14 to 22 nm.

The power spectral density (PSD) of the drain current S_{ID} was measured in the linear regime at V_{DS} = 200 mV to identify the dominant noise sources in the channel with these two *in situ* SiN passivation thicknesses. Noise measurements were carried out on devices under stationary conditions and were reproducible. At low frequency, S_{ID} varies as 1/f type spectra (in the 1 Hz to 1 kHz frequency range) and no generation-recombination noise components were observed.

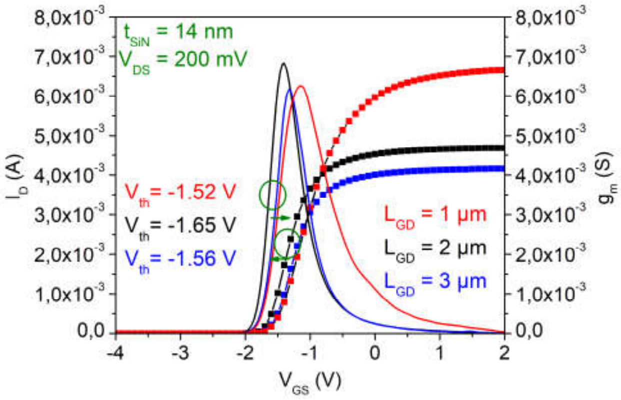


Fig. 2. I_D-V_{GS} and g_m-V_{GS} of InAlGaN/GaN MIS HEMTs with t_{SiN} = 14 nm and L_{GD} = 1, 2 and 3 µm at V_{DS} = 200 mV.

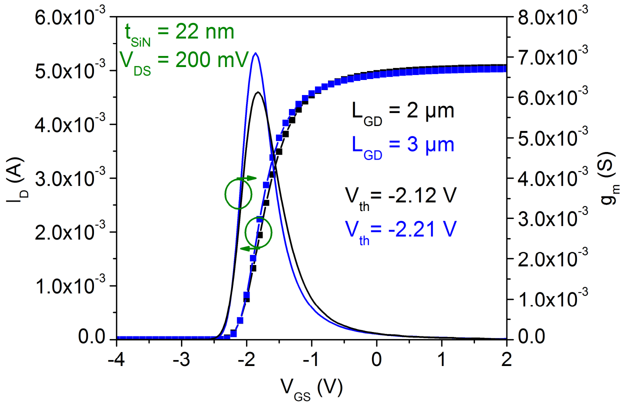


Fig. 3. I_D-V_{GS} and g_m-V_{GS} of InAlGaN/GaN MIS HEMTs with t_{SiN} = 22 nm and L_{GD} = 2 and 3 µm at V_{DS} = 200 mV.

The experimental points representing S_{ID}/I_D^2 versus gate overdrive voltage (V_{GS}-V_{TH}), in the linear regime (V_{DS} = 200 mV), of InAlGaN/GaN HEMTs with L_{GD} =1, 2 and 3 µm are shown in Fig.4. There is no significant impact of SiN thickness on the noise performance. S_{ID}/I_D^2 decreases with the gate overdrive as $(V_{GS}-V_{TH})^{-3}$. Similar S_{ID}/I_D^2 dependence over V_{GS}-V_{TH} indicating the dominant channel noise is located under the gate, as reported in previous works on GaAs MODFETs [25] and AlGaN/GaN HEMTs [26]. In agreement with these results, it can be pointed out that the current collapse level within these devices as assessed by pulsed measurements has been found to be similar regardless of the SiN cap layer thickness.

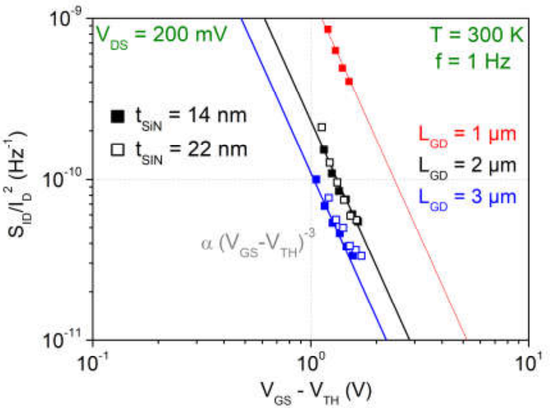


Fig. 4. Dependence of the relative PSD of the drain current S_{ID}/I_D^2 on the gate overdrive (V_{GS}-V_{TH}) at f = 1 Hz, V_{DS} = 200 mV and T = 300 K.

We previously analyzed S_{ID}/I_D^2 dependence over the gate-drain spacing of InAlGaN/GaN MIS-HEMTs by considering two noise sources in the channel: channel noise under the gate and channel noise in the gate-drain access regions [27].

Here, the source and drain contact resistances and the gate-source access region resistance are negligible, hence the noise sources of these resistances are not considered in the model. Following the procedure of [27], the experimental data representing the relative drain current channel noise under the gate (S_{IRCH}/I_D^2) versus gate overdrive voltage (V_{GS}-V_{TH}), in the linear regime (V_{DS} = 200 mV), of InAlGaN/GaN HEMTs with L_{GD} = 1, 2 and 3 µm are shown in Fig.5. The relative drain current channel noise under the gate S_{IRCH}/I_D^2 decreases with the gate overdrive as $(V_{GS}-V_{TH})^{-3}$ with no significant impact of L_{GD}. Similar dependence over V_{GS}-V_{TH} indicating the dominant channel noise is located under the gate, as reported in previous works [25,26]. In [27], the channel noise under the gate was also the main contribution of the total channel noise for for low gate-drain access region spacing L_{GD} < 10 µm.

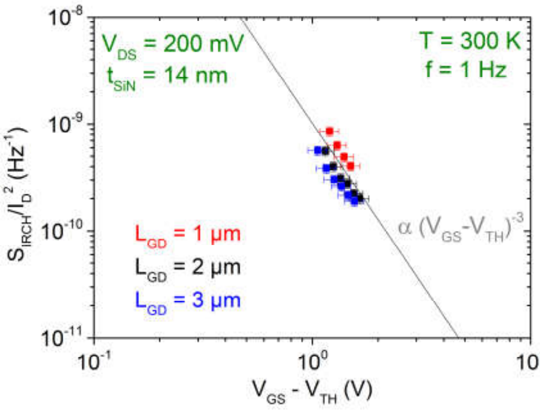


Fig. 5. Dependence of the relative drain current channel noise under the gate S_{IRCH}/I_D^2 on the gate overdrive (V_{GS}-V_{TH}) at f = 1 Hz, V_{DS} = 200 mV and T = 300 K.

IV. CONCLUSION

The low frequency noise of sub-10 nm quaternary barrier layer InAlGaN/GaN HEMTs with two different MOVPE *in situ* SiN passivation thicknesses and ultra-short gate was studied. The low frequency noise is not impacted by the *in situ* SiN thickness and shows a high InAlGaN/GaN interface quality. The S_{ID}/I_D^2 dependence over V_{GS}-V_{TH} indicates that the dominant channel noise is located under the gate. Sub-10 nm InAlGaN quaternary barrier combined with *in situ* SiN passivation layer are promising to enhance the performance of GaN based HEMTs.

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